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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,745	10/26/2001	Kang-yoon Lee	5649-925	2804

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EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,745	LEE ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-21 and 31-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-21 and 31-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's arguments with respect to claims 10-21 and 31-46 have been considered but are moot in view of the new ground(s) of rejection.

Inventorship

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 10-13, 15-18, 31-32, 36 and 39-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Isobe (U.S. 6,417,047 B1).

Isobe discloses a method of forming a semiconductor device with

(10); (15); (31) forming a trench (34) in a substrate (31) (see Figure 1B);

forming an isolation layer (35) in the trench (34) so as to cover a first sidewall portion of the trench (34) (see Figures 1C and 2B);

forming a gate electrode (36) on a second sidewall portion of the trench (34) (see column 2, lines 31-58. Figures 1C and 2B);

(11) wherein forming the gate electrode comprises: forming a gate insulating layer (37) on the second sidewall portion of the trench; forming the gate electrode (38) on the gate insulating layer (37) (see Figure 2B);

(12) wherein forming the isolation layer comprises: forming a buffer layer in the trench; and forming the isolation layer on the buffer layer in the trench (see Figures 8G-8H);

(13) wherein forming the isolation layer comprises: forming a liner layer on the buffer layer; and forming the isolation layer on the liner layer in the trench (see Figures 8G-8H);

(16) wherein the etching step comprises: forming an oxide layer on the substrate; forming a mask on the oxide layer; patterning the mask to expose at least a portion of the oxide layer; etching the exposed portion of the oxide layer and the substrate to form the trench and the mesa (see Figures 8A-8C);

(17) wherein filling the trench with the insulating material comprises: filling the trench with the insulating material so as to cover the mask; planarizing the insulating material until a surface of the mask is exposed; patterning the insulating material so that the mask extends through a surface of the insulating material; etching the mask to substantially remove the mask from the upper surface of the mesa; etching the insulating material so that the insulating material covers the first portion of the sidewall and exposes the second portion of the sidewall (see Figures 8A-8K);

(18) forming a buffer layer in the trench before filling the trench with the insulating material; thermally treating the insulating material after filling the trench with the insulating material (see Figure 8G);

(32) further comprising the step of forming a buffer layer at the interface between the isolation layer and the trench (see Figure 8G-8H);

(36) wherein the step of forming the trench comprises the steps of: forming a pad oxide layer on the semiconductor substrate; forming a mask on the pad oxide layer; etching the semiconductor substrate using the mask as an etching mask, and the step of forming the isolation layer comprises the steps of: forming a filling layer which fills the trench; chemically and mechanically polishing the filling layer so as to expose the surface of the mask; etching the surface of the polished filling layer exposed by the mask; removing the mask; etching the resultant filling layer so as to expose the upper sidewalls of the trench (see Figures 8A-8K);

(39) wherein the gate electrode covers the upper sidewalls of the trench and the surface of the isolation layer and is formed on the gate insulating layer which is interposed between the gate electrode and the upper surface of the semiconductor substrate (see Figure 2B).

(40) forming a trench (34) "mesa structure" having sidewalls and a top surface in a substrate (31) (see Figures 1C and 2B);

forming a gate electrode (36) on the trench (34) "mesa structure" that extends across the top surface and down respective upper portions of the sidewall (see column 2, lines 31-58. Figures 1C and 2B);

(41) wherein forming the gate electrode comprising: forming a gate insulating on respective upper portions of the sidewall; forming a gate electrode (36) on the gate insulating layer (see column 2, lines 31-58. Figures 1C and 2B);

(42) forming an isolation layer comprising an insulating material on respective lower portions of the sidewall (see column 2, lines 31-58. Figures 1C and 2B);

(43) wherein forming the mesa structure comprising: forming a pair of trenches on opposing sides of the mesa structure; and wherein forming the isolation layer comprising: forming the isolation layer in the respective trenches so as to cover the respective lower portions of the sidewall (see Figures 8H-8I);

(44) wherein forming the isolation layer further comprises: forming a buffer layer (106) in the respective trenches; forming the isolation layer(107) on the buffer layer in the respective trenches (see Figures 8G-8H);

(45) wherein forming the isolation layer further comprises: forming a liner layer on the buffer layer; forming the isolation layer on the liner layer in the respective trenches (see Figures 8G-8H);

(46) forming an impurity layer in the top surface and the respective upper portions of the sidewall (see column 6, lines 32-55. Figure 8C);

Claims 14 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isobe (U.S. 6,417,047 B1) in view of Hisamoto et al. (U.S. 5,246,877)

Isobe teaches everything above but fails to forming an impurity layer in the second sidewall portion of the trench. However, Hisamoto discloses a method of manufacturing a semiconductor device with **(14)** further comprising: forming an impurity layer in the second sidewall portion of the trench (see column 3, lines 23-30); **(19)** implanting ion impurities in the second portion of the sidewall and the upper surface before forming the gate electrode (see column 3, lines 23-30. Figure 3); **(20)** wherein implanting ion impurities comprises: implanting ion impurities at an oblique angle with

respect to a plane formed by a non-etched portion of the substrate in the second portion of the sidewall and the upper surface (see column 3, lines 23-30); **(21)** wherein forming the gate electrode comprises: forming an oxide layer on the second portion of the sidewall and the upper surface; implanting ion impurities through the oxide layer in the second portion of the sidewall and the upper surface; etching the oxide layer; forming the gate electrode on the second portion of the sidewall and the upper surface (see Figure 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Isobe and Hisamoto to fabricate a semiconductor device to exceed its performance criteria.

Claims 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isobe (U.S. 6,417,047 B1) in view of Witek et al. (U.S. 6,146,970)

Isobe discloses everything above but fails to wherein the surface of the isolation layer is lower than the upper surface of the semiconductor substrate; wherein the step of forming the isolation layer comprising the steps of: forming a filling layer which fills the trench; etching the filling layer to a predetermined thickness so as to expose the upper sidewalls of the trench. However, Witek discloses a method for forming acapped shallow trench isolation structure with **(34)** wherein the surface of the isolation layer is lower than the upper surface of the semiconductor substrate (see Figure 10); **(35)** wherein the step of forming the isolation layer comprising the steps of: forming a filling layer which fills the trench; etching the filling layer to a predetermined thickness so as to expose the upper sidewalls of the trench (see Figures 9-10). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to combine the above teachings to make a semiconductor device to exceed its performance criteria.

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isobe (U.S. 6,417,047 B1) in view of Noble (U.S. 6,403,429 B2).

Isobe teaches everything above except for further comprising the step of forming an impurity layer to control threshold voltage beneath the surface of the upper sidewalls of the trench and beneath the upper surface of the semiconductor substrate before the step of forming the gate insulating layer. However, Noble discloses a method of forming an electrical connection in an integrated circuit with **(37)** further comprising the step of forming an impurity layer to control threshold voltage beneath the surface of the upper sidewalls of the trench and beneath the upper surface of the semiconductor substrate before the step of forming the gate insulating layer (see column 7, lines 26-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the above teachings to fabricate a semiconductor device to exceed its performance criteria.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isobe (U.S. 6,417,047 B1) in view of Noble (U.S. 6,403,429 B2) and further in view of Rodder et al. (U.S. 6,306,712 B1)

Isobe and Noble teach the above outlined features except for wherein the impurity layer is formed using angle implantation. Furthermore, Rodder discloses a

method for forming a transistor with **(38)** wherein the impurity layer is formed using angle implantation (see column 4, lines 35-40. Figure 2C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Isobe, Noble and Rodder to angled implant during a fabricating process of a semiconductor device to exceed its performance criteria.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isobe (U.S. 6,417,047 B1) in view of Kim (U.S. 6,339,004 B1)

Isobe discloses everything above except for further comprising the step of forming a liner of a silicon nitride layer at the interface between the buffer layer and the isolation layer. However, Kim discloses a method of forming shallow trench isolation with **(33)** further comprising the step of forming a liner of a silicon nitride layer at the interface between the buffer layer and the isolation layer (see column 3, lines 7-19. Figures 2B-2C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Isobe and Kim to manufacture a semiconductor device to exceed its performance criteria.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

C. Eckhart
CARROLL EVERHART
PRIMARY EXAMINER

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June 2, 2003